IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Atty. Docket

ADRIANUS VAN BEZOOIJEN ET AL NL 000640

Serial No.

Filed: CONCURRENTLY

DC-OFFSET CORRECTION CIRCUIT HAVING A DC CONTROL LOOP AND A DC BLOCKING CIRCUIT

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

3. (Amended) A receiver (1) comprising the DC-offset correction circuit (I1, Q1) according to claim 1, characterised in that the receiver (1) comprises channel filter means (DFI, DFQ) coupled between the summing device (9-1, 9-2) and the DC blocking circuit (17-1, 17-2).

5. (Amended) The receiver (1) according to claim 3, characterised in that the receiver is a quadrature receiver (1).

6. (Amended) The receiver (1) according to claim 3, characterised in that the receiver is a low-IF receiver, or a zero-IF receiver.

7. (Amended) The receiver (1) according to claim 3, characterised in that the receiver is a double conversion receiver (1).

8. (Amended) The receiver (1) according to claim 3, characterised in that the receiver (1) is provided with analog to digital (AD) converters (13-1, 13-2) and/or digital to analog (DA) converters (16-1, 16-2; 20).

9. (Amended) The receiver (1) according to claim 3, characterised in that the receiver (1) is provided with switchable means (3, 5, 7-1, 7-2).

REMARKS

The foregoing amendments to claims 3 and 5-9, were made solely to avoid filing the claims in the multiple dependent form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights he may have under the Doctrine of Equivalents. Applicant furthermore reserves his right to reintroduce

subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

By_______________________

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APPENDIX

3. (Amended) A receiver (1) comprising the DC-offset correction circuit (I1, Q1) according to claim 1 ~~or claim 2~~, characterised in that the receiver (1) comprises channel filter means (DFI, DFQ) coupled between the summing device (9-1, 9-2) and the DC blocking circuit (17-1, 17-2).

5. (Amended) The receiver (1) according to claim 3 ~~one of the claims 3-4~~, characterised in that the receiver is a quadrature receiver (1).

6. (Amended) The receiver (1) according to claim 3 ~~one of the claims 3-5~~, characterised in that the receiver is a low-IF receiver, or a zero-IF receiver.

7. (Amended) The receiver (1) according to claim 3 ~~one of the claims 3-6~~, characterised in that the receiver is a double conversion receiver (1).

8. (Amended) The receiver (1) according to claim 3 ~~one of the claims 3-7~~, characterised in that the receiver (1) is provided with analog to digital (AD) converters (13-1, 13-2) and/or digital to analog (DA) converters (16-1, 16-2; 20).

9. (Amended) The receiver (1) according to claim 3 ~~one of the claims 3-8~~, characterised in that the receiver (1) is provided with switchable means (3, 5, 7-1, 7-2).